Remarks

Claims 1, 3-8, and 10-20 are pending in this application. Claims 2 and 9 have been cancelled herein. Claims 1, 7, 10, and 17 have been amended. The Examiner has rejected claims 1, 2 and 4-6 under 35 U.S.C. § 102(a) as being anticipated by U.S. Publication No. 2003/0046464 to Murty et al. (hereinafter "Murty"). Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Murty in view of U.S. Patent No. 5,809,314 to Carmean et al. (hereinafter "Carmean"). Further, claims 7-15, 17, 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Murty in view of U.S. Patent No. 6,857,084 to Giles (hereinafter "Giles"). Finally, claims 16 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Murty in view of Giles and further in view of Carmean.

A. Claims rejected under 35 U.S.C. 102

Claims 1, 2, 4, 5, and 6 are rejected under 35 U.S.C. 102(a) as being anticipated by Murty. Because the Examiner rejected independent claim 1 under section 102(b) on the basis of Murty, each element of the claim must be disclosed in Murty. Murty, however, does not disclose each element of independent claim 1, as amended. Specifically, Murty does not disclose the claimed element of the processors being operable to be serially released from the interrupt mode according to a **predetermined time delay** following the release of each successive processor from the interrupt mode.

In accordance with the present invention, the processors exit from the interrupt mode on a serial basis according to a **time delay managed** by the interrupt handling processor. (Summary, page 4, lines 16-18). Because the processors exit interrupt mode on the basis of a time-delayed release, the contention by the processors for resources of the computer system is reduced or eliminated, allowing the computer system to more quickly complete interrupt-related tasks. (Specification, page 4, lines 18-21) Accordingly, claim 1, as amended, discloses an information handling system where the interrupt handling processor releases the non-interrupt handling processors serially from the interrupt handling mode according to a **predetermined time delay**, thereby **reducing** the **contention** by the processors for resources of the computer system.

On the other hand, Murty discloses a multi processor system wherein the first logical processor to access the shared register handles the common interrupt and the non-interrupt handling processors must **vie for a shared resource**, namely an interrupt claim register (ICR). Murty states, "In response to a common interrupt, the logical processors vie for access to a shared register." (Murty, Abstract). Thus, Murty is not concerned with reducing the contention by the processors for a shared resource of the computer system, as Murty specifically states that these processors must vie (or contend) for a shared resource. Additionally, Murty fails to teach or disclose releasing non-interrupt handling processors serially from the interrupt handling mode according to a **predetermined time delay.** The Examiner points to paragraph [0046] of Murty as teaching this limitation. However, this paragraph states only that the mechanisms for resetting the single flag of Murty "assume that the time between common interrupts is typically greater than the time necessary for all of the logical processors to execute the interrupt handler (or portions thereof) and access the flag." (Murty, [0046]) First, this passage only states that Murty **assumes** a fact about the time between common interrupts, which is not the same as having a **predetermined** time delay. Second, the time discussed in this passage is the time **between interrupts**, and **not** the **time delay** between releasing non-interrupt handling processors. Finally, when Murty does mention the time necessary for the processors to execute the interrupt handler, it is only with reference to an **aggregate** amount of time required for **all** of the processors to perform a task, and this in no way teaches or discloses a **predetermined time delay** between releasing non-interrupt processors serially from the interrupt handling mode.

Because Murty fails to disclose the claimed element of the processors being operable to be serially released from the interrupt mode according to a **predetermined time delay** following the release of each successive processor from the interrupt mode, Murty fails to support a finding of anticipation under 35 U.S.C. 102(b). Applicant requests that this rejection be withdrawn. Claims 3-6 depend directly or indirectly from independent claim 1 and are therefore allowable for at least the same reason.

B. Claims rejected under 35 U.S.C. 103

Claims 7-15, 17, 19, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murty in view of Giles. Independent claims 7 and 17 recite a method for exiting from an interrupt mode in a multiple processor computer system comprising setting an indicator **associated with the respective processor** to identify that the respective processor is in an interrupt mode. Murty fails to teach or suggest setting an indicator **associated** with the **respective** processor to identify that the respective processor is in an interrupt mode. Murty, at best, teaches a "race-to-flag" type mechanism in which **a single flag** exists in a register, for example, that is accessible by **all** of the logical processors. (Murty, [0034]) Additionally, this flag is used by a processor to "determine whether or not it is responsible for handling the common interrupt." (Murty, [0034]) The flag does not identify that a given processor is in an interrupt mode, rather, the single flag for **all** of the processors is used to **determine** whether *any* processor reading the flag is responsible or not for handling an interrupt. The flag does not provide individual information regarding the status of each processor as does the invention of the present application. Additionally, Giles fails to remedy this deficiency of Murty. Giles, at best, teaches that processors enter a debug mode as a result of one processor asserting a **single** debug **event signal**. (Giles, Abstract). Thus, Giles does not teach or suggest setting an indicator associated with each respective processor to identify that the respective processor is in an interrupt mode.

Thus, the combination of Murty and Giles fails to teach or suggest setting an indicator **associated with the respective processor** to identify that the respective processor is in an interrupt mode. Because all of the elements of independent claims 7 and 17 are not taught or suggested by the combination of Murty and Giles, a prima facie case of obviousness is not established. In order to establish a prima facie case of obviousness, the references cited by the Examiner must disclose all claimed limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974). Here, regardless of whether it is proper to combine the teachings of Murty and Giles, all of the claimed limitations of independent claims 7 and 17 are not shown in the combination. Applicant respectfully submits that the rejection of claims 7 and 17 should be withdrawn and that these claims should be passed to issuance. Claims 8-16 and 18-20 depend directly or indirectly from independent claims 7 and 17 and are therefore requested to be passed to issuance for at least the same reasons.

Conclusion

Applicant respectfully submits that claims 1, 3-8, and 10-20 should be passed to issuance.

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